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Jameco Part Number 171811

MOTOROLA

SN54/74LS669

SYNCHRONOUS 4-BIT UP/DOWN COUNTER

SYNCHRONOUS 4-BIT UP/DOWN COUNTER

LOW POWER SCHOTTKY

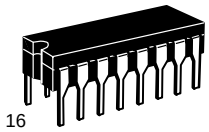
The SN54/74LS669 is a synchronous 4-bit up/down counter. The LS669 is a 4-bit binary counter. For high speed counting applications, this presettable counter features an internal carry lookahead for cascading purposes. By clocking all flip-flops simultaneously so the outputs change coincident with each other (when instructed to do so by the count enable inputs and internal gating) synchronous operation is provided. This helps to eliminate output counting spikes, normally associated with asynchronous (ripple-clock) counters. The four master-slave flip-flops are triggered on the rising (positive-going) edge of the clock waveform by a buffered clock input.

Circuitry of the load inputs allows loading with the carry-enable output of the cascaded counters. Because loading is synchronous, disabling of the counter by setting up a low level on the load input will cause the outputs to agree with the data inputs after the next clock pulse.

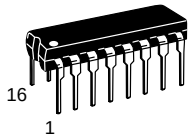
Cascading counters for N-bit synchronous applications are provided by the carry look-ahead circuitry, without additional gating. Two count-enable inputs and a carry output help accomplish this function. Count-enable inputs (P and T) must both be low to count. The level of the up-down input determines the direction of the count. When the input level is low, the counter counts down, and when the input is high, the count is up. Input T is fed forward to enable the carry output. The carry output will now produce a low level output pulse with a duration ≈ equal to the high portion of the Q_A output when counting up and when counting down ≈ equal to the low portion of the Q_A output. This low level carry pulse may be utilized to enable successive cascaded stages. Regardless of the level of the clock input, transitions at the P or T inputs are allowed. By diode-clamping all inputs, transmission line effects are minimized which allows simplification of system design.

Any changes at control inputs ($\overline{\text{ENABLE P}}$, $\overline{\text{ENABLE T}}$, LOAD, UP/DOWN) will have no effect on the operating mode until clocking occurs because of the fully independant clock circuits. Whether enabled, disabled, loading or counting, the function of the counter is dictated entirely by the conditions meeting the stable setup and hold times.

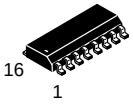
- Programmable Look-Ahead Up/Down Binary/Decade Counters
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

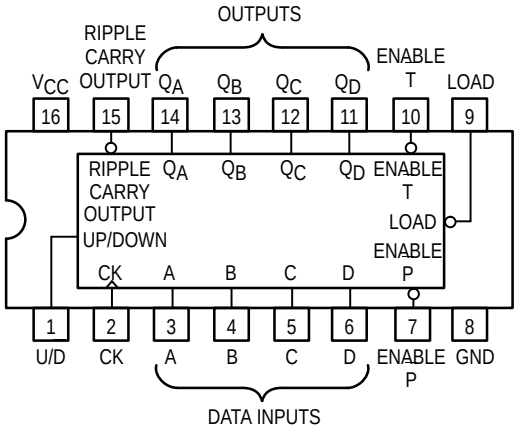


D SUFFIX
SOIC
CASE 751B-03

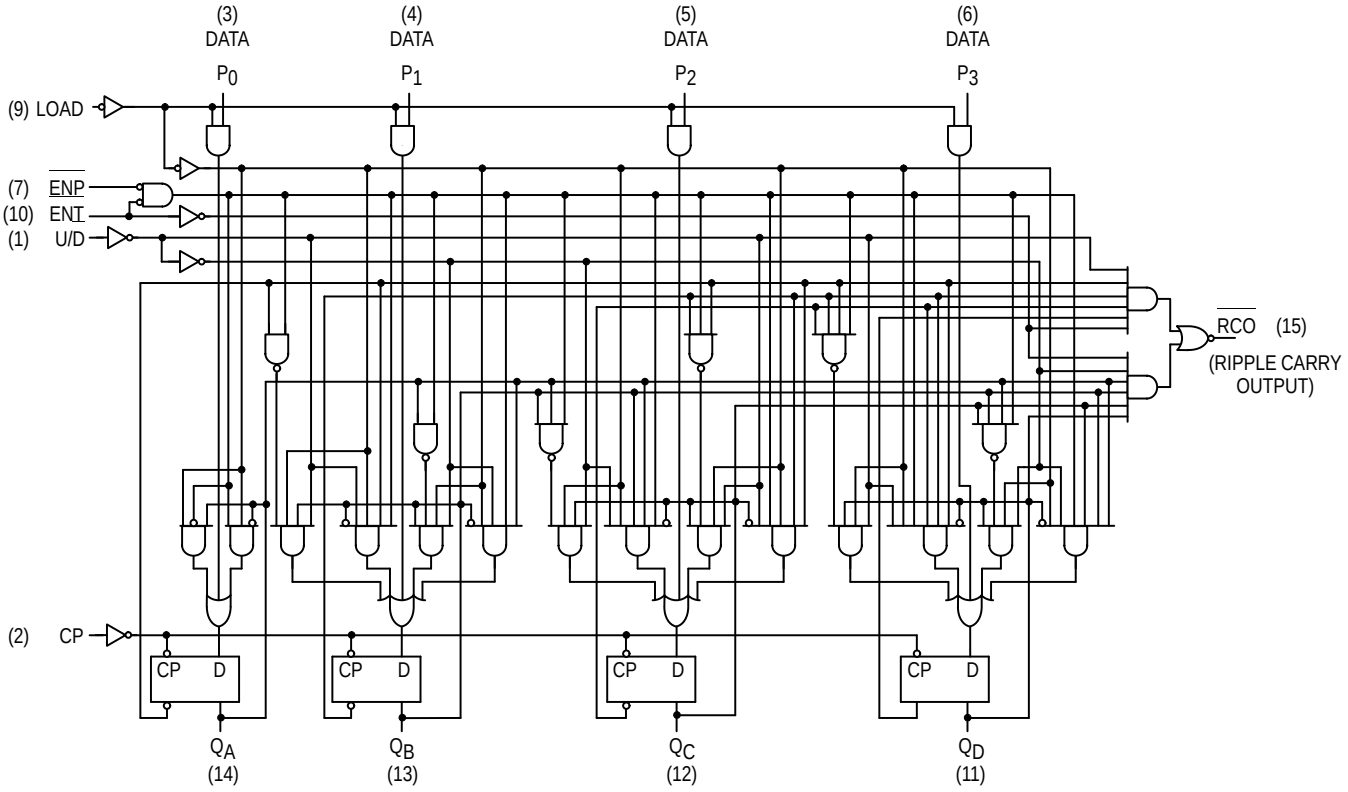
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM (TOP VIEW)



LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	Others			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		Enable T			40	µA		
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		Enable T			0.2	mA		
I_{IL}	Input LOW Current	Others			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Enable T			–0.8	mA		
I_{OS}	Short Circuit Current (Note 1)		–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

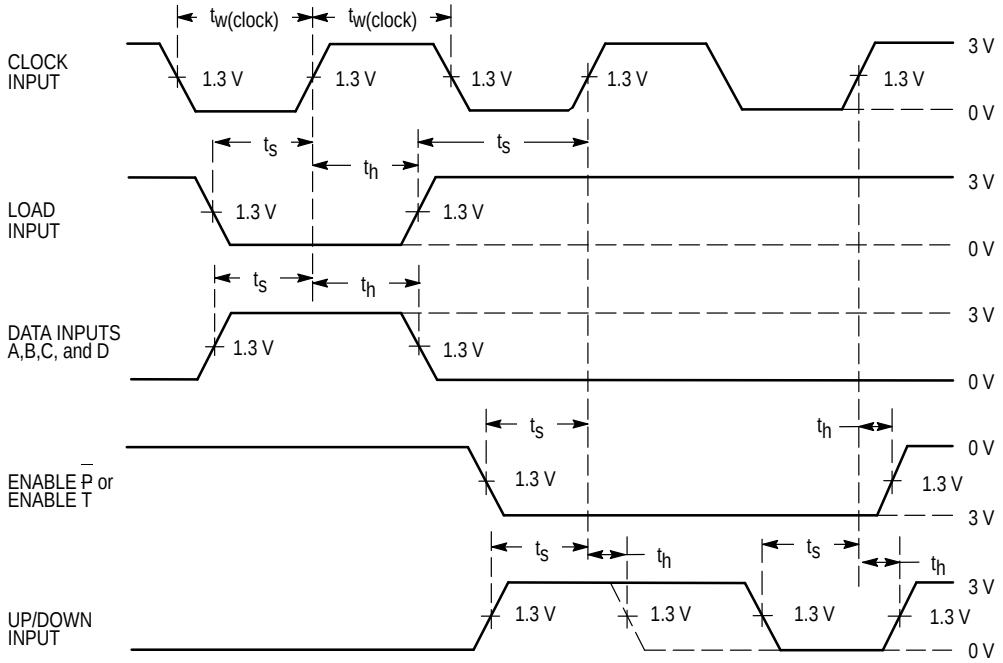
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	32		MHz	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to RCO		26 40	40 60	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Any Q		18 18	27 27	ns	
t_{PLH} t_{PHL}	Enable to $\overline{RCO}$		11 29	17 45	ns	
t_{PLH} t_{PHL}	$U/\overline{D}$ to $\overline{RCO}$		22 26	35 40	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_W	Clock Pulse Width	20			ns	V_{CC} = 5.0 V
t_S	Data Setup Time	20			ns	
t_S	Enable Setup Time	35			ns	
t_S	$\overline{Load}$ Setup Time	25			ns	
t_S	$U/\overline{D}$ Setup Time	30			ns	
t_h	Hold Time, Any Input	0			ns	

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS